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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/764,150	01/23/2004	Dennis E. Dudeck	1-4-32-5	8145

7590 05/03/2006

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EXAMINER	
NGUYEN, TAN	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 05/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/764,150	DUDECK ET AL.	
	Examiner	Art Unit	
	Tan T. Nguyen	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16-21* is/are pending in the application.

4a) Of the above claim(s) *1-15 and 22-26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16,17,19 and 20* is/are rejected.

7)☒ Claim(s) *18 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The Response to Restriction Requirement submitted by Applicants on April 13, 2006 has been received.

2. Claims 1-15 and 22-26 have been withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on April 13, 2006.

3. Applicant's election with traverse of Group II, claims 16-21 in the reply filed on April 13, 2006 is acknowledged. The traversal is on the ground(s) that "each Group is redirection of leakage current in memory devices, and it is believed that a complete search for each Group would require a search of most, if not all, of the individual classes and subclasses", and "an examination of both Groups would not imposed a serious burden on the Examiner". This is not found persuasive because the examination of both Groups would impose a serious burden on the Examiner because although both of the Groups have similar purpose that is to reduce the leakage current in the memory devices, but how the methods and the device to achieve the purpose in each Group is different from the other. The first Group reduce the leakage current in the ROM by terminates the precharge phase independent of the clock edge, while the second reducing the leakage current by not precharging the memory device in the standby mode. The memory device terminates independent of the clock edge and not precharged during standby mode are completely different inventions.

The requirement is still deemed proper and is therefore made FINAL.

4. The indicated allowability of claims 16-21 is withdrawn in view of the newly discovered reference(s) to Ashizawa (U.S. Patent No. 6,990034) Rejections based on the newly cited reference(s) follow.

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 16 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ashizawa (U.S. Patent No. 6,990034).

Ashizawa disclosed in Figure 1 a memory device [1] having a plurality of SRAMs (column 4, line 43-44). A control circuit [3] generates various control signals, more specifically, a control signal (operational mode control signal) [SM] which control the standby mode of SRAMs [4,5]. The control signal [SM] controls the SRAMs [4,5] to the standby mode at high level, and to read or write mode at low level (column 4, line 48-58). The control signal [SM] outputted from the control signal generation circuit [3] is input to a memory control circuit [12] of the SRAM [4]. A precharge cancel signal [Ø] is outputted from a precharge control circuit (NAND gate [20] and inverter [21]) based on the control signal {SM] and a bit line control signal [EQ} from an internal clock/control signal generation circuit [11] (column 5, lines 25-45).

Ashizawa showed in Figure 2 the waveform chart of the operation of memory device 1. The normal operation mode (read mode or write mode) is set before time [t4], and the

standby mode is set from time [t4]. At time [t1], the bit line pair [BL], [XBL] are precharged to high level (column 6, lines 16-25). At the time [t4], the precharge cancel signal [Ø] changes to high level to turn off the p-MOSFETs [30]. For this reason, the precharge of bit lines [BL], [XBL] is canceled, and the bit lines [BL], [XBL] are set in the floating state. With the above operation, the SRAM [4] can reduce the leakage current by setting the bit lines [BL], [XBL] in the floating state.

Ashizawa did not discuss a read only memory device.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the memory device of Ashizawa by replacing the SRAM of Ashizawa with read only memory device.

The rationale is as follows: A person of ordinary skill in the art would have been motivate to use the read only memory device to avoid lost of data when the power supply is removed, and still reduces the leakage current of the read only memory device during standby mode.

Regarding claims 17 and 20, Ashizawa disclosed at time [t2], the bit line control signal [EQ] and the precharge cancel signal [Ø] are changed to high level to turn off the p-MOSFETs [30], precharge of bit lines [BL] and [XBL] is canceled (column 6, lines 30-35). The bit line control signal [EQ] and the precharge cancel signal [Ø] would be considered as the clock signals.

7. Claims 18 and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Furutani and Miyashita et al. are cited to show precharge voltage is disconnect to the bit lines during standby mode.

The prior art failed to show or suggest the limitation of the precharge phase is internally timed out prior to a subsequent clock edge.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tan T. Nguyen whose telephone number is (571) 272-1789. The examiner can normally be reached on Monday to Friday from 07:00 AM to 03:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian, can be reached at (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tan T. Nguyen
Primary Examiner
Art Unit 2827
April 28, 2006